A cont.

preparing a first substrate having a nonporous monocrystalline semiconductor layer on a monocrystalline semiconductor substrate with the interposition of a porous layer, said first substrate having two opposing faces;

bonding a second substrate, said second substrate having two opposing faces, to said first substrate to yield a multilayer structure where said nonporous monocrystalline semiconductor layer is arranged inside; and

separating the multilayer structure at said porous layer such that said nonporous monocrystalline semiconductor layer remains on said second substrate.

23. The process according to claim 25, wherein said step of separating said multilayer structure is conducted by applying a tensile force to said multilayer structure in a direction perpendicular to the faces of said first and second substrates.

24. The process according to claim 25, wherein said step of separating said multilayer structure is conducted by applying a compression force to said multilayer structure in a direction perpendicular to the faces of said first and second substrates.

25. The process according to claim 25, wherein said step of separating said multilayer structure is conducted by applying a shearing force to said multilayer

A' cont.

structure in a direction parallel to the faces of said first and second substrates.

26. The process according to claim 25, wherein said step of separating said multilayer structure is conducted by applying a wave energy to said multilayer structure to break said porous layer.

27. The process according to claim 29, wherein said wave energy is ultrasonic.

28. The process according to claim 25, wherein said step of separating said multilayer structure is conducted by inserting a sharp blade into said porous layer of said multilayer structure.

29. The process according to claim 25, wherein said step of separating said multilayer structure is conducted by impregnating a liquid into said porous layer of said multilayer structure, followed by heating or cooling said multilayer structure such that the liquid expands.

30. The process according to claim 25, wherein said step of separating said multilayer structure is conducted by beginning to etch selectively said porous layer at the edge of said multilayer structure.

A' cont.

31. The process according to claim 25, wherein said step of separating said multilayer structure is conducted such that a portion of said porous layer remains together with said nonporous monocrystalline semiconductor layer on said second substrate and further comprises removing the portion of said porous layer from said second substrate where the separation has been carried out.

32. The process according to claim 34, wherein said step of removing the portion of said porous layer is conducted by etching the portion of said porous layer on said second substrate such that said nonporous monocrystalline semiconductor layer remains.

33. The process according to claim 34, wherein said step of removing the portion of said porous layer is conducted by grinding the portion of said porous layer on said second substrate such that said nonporous monocrystalline semiconductor layer remains.

34. The process according to claim 25, wherein said step of separating said multilayer structure is conducted such that a portion of said porous layer is not removed from said semiconductor substrate, followed by removing the portion of said porous layer remaining on said semiconductor substrate.

d'cont.

35. The process according to claim 37, wherein said process is further comprised of flattening a surface of said monocrystalline semiconductor substrate where the portion of said porous layer has been removed.

36. The process according to claim 25, wherein said first substrate is formed by making a portion of a silicon substrate porous to form a porous layer, and epitaxially growing a nonporous monocrystalline semiconductor layer on said porous layer.

37. The process according to claim 39, wherein said silicon substrate portion is made porous by anodization.

38. The process according to claim 40, wherein current density is altered in stages when said anodization is carried out.

39. The process according to claim 39, wherein said epitaxial growth is conducted by a method selected from a group consisting of a molecular beam epitaxy method, a plasma CVD method, a reduced pressure CVD method, a photo-assisted CVD method, a bias sputtering method, and a liquid-phase epitaxial growth method.

A' cont.

40. The process according to claim 25, wherein said nonporous monocrystalline semiconductor layer is comprised of a monocrystalline silicon layer.

41. The process according to claim 25, wherein said nonporous monocrystalline semiconductor layer is comprised of a monocrystalline compound semiconductor layer.

42. The process according to claim 44, wherein said monocrystalline compound semiconductor layer is comprised of a GaAs layer or an AlGaAs layer.

43. The process according to claim 25, wherein said porous layer is comprised of plural layers of different porosity.

44. The process according to claim 25, wherein said first and second substrates are bonded through an insulating layer.

45. The process according to claim 47, wherein said insulating layer is comprised of an oxidized film formed by oxidizing a surface of said nonporous monocrystalline semiconductor layer.

d'cont.

46. The process according to claim 47, wherein said insulating layer is comprised of an insulating thin plate, and said first and second substrates are bonded with the interposition of said plate to form a three layer structure.

47. The process according to claim 47, wherein said insulating layer is comprised of a SiO_2 layer formed on said second substrate.

48. The process according to claim 25, wherein said second substrate is comprised of a silicon substrate.

49. The process according to claim 25, wherein said second substrate is a light transmissive substrate.

50. The process according to claim 52, wherein said second substrate is a quartz substrate or a glass substrate.

51. A process for producing a semiconductor substrate comprising the steps of:

preparing a first substrate having two nonporous monocrystalline semiconductor layers located on the respective sides of a monocrystalline semiconductor with the interposition of respective porous layers, said first substrate having two opposing faces;

A' cont.

bonding two second substrates to the respective faces of said first substrate to yield a multilayer structure, each of said second substrates having two opposing faces; and

separating the multilayer structure at each of said two porous layers such that said two nonporous monocrystalline semiconductor layers exist on each of said respective two second substrates.

52. The process according to claim 54, wherein said step of separating said multilayer structure is conducted by applying a tensile force to said multilayer structure in a direction perpendicular to the faces of said first substrate and said two second substrates.

53. The process according to claim 54, wherein said step of separating said multilayer structure is conducted by impregnating a liquid into each of said two porous layers of said multilayer structure, followed by heating or cooling said multilayer structure to expand the liquid.

54. The process according to claim 54, wherein said step of separating said multilayer structure is conducted such that a portion of said porous layer remains together with said nonporous monocrystalline semiconductor

layer on each of said two second substrates and further comprises removing the portion of said porous layer from each of said two second substrates where the separation has been carried out.

55. The process according to claim 57, wherein said step of removing the portion of said porous layer is conducted by etching the portion of said porous layer on said two second substrates such that said nonporous monocrystalline semiconductor layer remains.

56. The process according to claim 57, wherein said step of removing the portion of said porous layer is conducted by grinding the portion of said porous layer on said two second substrates such that said nonporous monocrystalline semiconductor layer remains.

57. The process according to claim 54, wherein said step of separating said multilayer structure is conducted such that a portion of said porous layer is not removed from each side of said monocrystalline semiconductor substrate, followed by removing the portion of said porous layers remaining on both sides of said monocrystalline semiconductor substrate.

A'cont.

58. The process according to claim 60, wherein said process is further comprised of flattening respective surfaces of both sides of said monocrystalline semiconductor substrate where the portion of said porous layer has been removed.

59. The process according to claim 54, wherein said first substrate is formed by making both sides of a silicon substrate partially porous to form two porous layers, and subsequently epitaxially growing two nonporous monocrystalline semiconductor layers on each said two porous layers.

60. The process according to claim 62, wherein both sides of the silicon substrate are made porous by anodization.

61. The process according to claim 62, wherein said epitaxial growth is conducted by a method selected from a group consisting of a molecular beam epitaxy method, a plasma CVD method, a reduced pressure CVD method, a photo-assisted CVD method, a bias sputtering method, and a liquid-phase growth method.

A' cont.

62. The process according to claim 54, wherein said two nonporous monocrystalline semiconductor layers are comprised of two monocrystalline silicon layers.

63. The process according to claim 54, wherein said two second substrates are bonded to said first substrate through two insulating layers.

64. The process according to claim 66, wherein each of said two insulating layers in comprised of an oxidized film formed by oxidizing a surface of each of said two nonporous monocrystalline semiconductor layers.

65. The process according to claim 66, wherein each of said two insulating layers is comprised of an insulating thin plate, and said two second substrates are bonded to said first substrate with the interposition of said two insulating thin plates, to form a five layer structure.

66. The process according to claim 66, wherein each of said two insulating layers is comprised of a SiO_2 layer formed on each of said two second substrates.

67. The process according to claim 54, wherein said second substrate is comprised of a silicon substrate.

A' cont.

68. A process for producing a semiconductor substrate comprising the steps of:

preparing a first substrate having a monocrystalline semiconductor layer on a monocrystalline semiconductor substrate with the interposition of a layer having a lower mechanical strength than that of said monocrystalline semiconductor substrate, said first substrate having two opposing faces;

bonding a second substrate to said first substrate to yield a multilayer structure where said monocrystalline semiconductor layer is arranged inside, said second substrate having two opposing faces; and

separating the multi-layer structure at said layer having the lower mechanical strength such that said monocrystalline semiconductor layer exists on said second substrate.

69. The process according to claim 71, wherein said step of separating said multilayer structure is conducted by applying a tensile force to said multilayer structure in a direction perpendicular to the faces of said first and second substrates.

70. The process according to claim 71, wherein said step of separating said multi-layer structure is conducted by applying a compression force to said multi-layer

structure in a direction perpendicular to the faces of said first and second substrates.

71. The process according to claim 71, wherein said step of separating said multilayer structure is conducted by applying a shearing force to said multilayer structure in a direction parallel to the faces of said first and second substrates.

72. The process according to claim 71, wherein said step of separating said multilayer structure is conducted by applying a wave energy to said multilayer structure to break said layer having the lower mechanical strength.

73. The process according to claim 75, wherein said wave energy is ultrasonic.

74. The process according to claim 71, wherein said step of separating said multilayer structure is conducted by inserting a sharp blade into said layer having the lower mechanical strength of said multilayer structure.

75. The process according to claim 71, wherein said step of separating said multilayer structure is conducted by impregnating a liquid into said layer having the

lower mechanical strength of said multilayer structure, followed by heating or cooling said multi-layer structure to expand the liquid.

76. The process according to claim 71, wherein said step of separating said multilayer structure is conducted by beginning to etch selectively said layer having the lower mechanical strength at the edge of said multilayer structure.

77. The process according to claim 71, wherein said step of separating said multilayer structure is conducted such that a portion of said layer having the lower mechanical strength remains together with said monocrystalline semiconductor layer on said second substrate and further comprises removing the portion of said layer having the lower mechanical strength from said second substrate where the separation has been carried out.

78. The process according to claim 80, wherein said step of removing the portion of said layer having the lower mechanical strength is conducted by etching the portion of said layer having the lower mechanical strength above said second substrate such that said monocrystalline semiconductor layer remains.

79. The process according to claim 80, wherein said step of removing the portion of said layer having the lower mechanical strength is conducted by grinding the portion of said layer having the lower mechanical strength above said second substrate such that said monocrystalline semiconductor layer remains.

80. The process according to claim 71, wherein said step of separating said multilayer structure is conducted such that a portion of said layer having the lower mechanical strength is not removed from said semiconductor substrate, followed by removing the portion of said layer having the lower mechanical strength remaining on said semiconductor substrate.

81. The process according to claim 83 wherein said process further comprises flattening a surface of said monocrystalline semiconductor substrate where the portion of said layer having the lower mechanical strength has been removed.

82. The process according to claim 71, wherein said first substrate is formed by making a portion of a silicon substrate porous to form a layer having the lower mechanical strength, and epitaxially growing a

d'cont.

monocrystalline semiconductor layer on said layer having the lower mechanical strength.

83. The process according to claim 85, wherein the silicon substrate portion is made porous by anodization.

84. The process according to claim 86, wherein current density is altered in stages when said anodization is carried out.

85. The process according to claim 85, wherein said epitaxial growth is conducted by a method selected from a group consisting of a molecular beam epitaxy method, a plasma CVD method, a reduced pressure CVD method, a photo-assisted CVD method, a bias sputtering method, and a liquid-phase growth method.

86. The process according to claim 71, wherein said monocrystalline semiconductor layer is comprised of a monocrystalline silicon layer.

87. The process according to claim 71, wherein said monocrystalline semiconductor layer is comprised of a monocrystalline compound semiconductor layer.

a'cont.

88. The process according to claim 90, wherein said monocrystalline compound semiconductor layer is comprised of a GaAs layer or an AlGaAs layer.

89. The process according to claim 71, wherein said layer having the lower mechanical strength is comprised of plural layers of different porosity.

90. The process according to claim 71, wherein said first and second substrates are bonded through an insulating layer.

91. The process according to claim 93, wherein said insulating layer is comprised of an oxidized film formed by oxidizing a surface of said monocrystalline semiconductor layer.

92. The process according to claim 93, wherein said insulating layer is comprised of an insulating thin plate, and said first and second substrates are bonded with the interposition of said plate to form a three layer structure.

93. The process according to claim 93, wherein said insulating layer is comprised of a SiO_2 layer formed on said second substrate.